REMARKS

Claims 1-13 and 15-17 are currently active.

The Examiner has objected to the drawings because the Examiner interprets figures 1, 4a and 4b are in contradiction with the definitions in the specification. Applicants respectfully traverses rejection. The figures are not in contradiction, but are consistent with the specification. For instance, in regard to figure 1, all that is showing is that the aggregator has a connection with the striper, as does the aggregator of each fabric, and that there is also a connection from the aggregator 11 to each memory controller in the fabric. There is no statement whatsoever that the lines represent a single data stream. That is not the case at all. The striper, performs as described in the specification and sends the stripe of the fragments to each respective fabric. This is shown in figure 1. Each aggregator of each fabric in communicate with each memory controller of each fabric. Similarly, each separator is in communication with each memory controller of the fabric in which it is in. Each separator of these fabrics is also in communication with the unstriper, which takes each of the corresponding stripes are fabrics and combines them to recreate the packet. That is all that the figures represent, and it is submitted the examiner is reading representations into the figures that are not present. Accordingly, the figures are proper.

The Examiner has rejected Claims 1-11 under 35 U.S.C. 112, first paragraph. The Examiner contends that the phrase "stripes of fragments" from claim 1 is not supported in the specification. Applicants respectfully traverses rejection.

The Examiner's attention is directed to the originally filed specification, page 10 beginning on line 25. Therein the specification states that the switch uses RAID techniques to increase overall switch bandwidth while minimizing individual fabric bandwidth. When RAID techniques are used, data from packets is fragmented and sent as stripes to different fabrics, with a parity fabric present so that if any one fabric fails and the stripe back been to the fabric is lost, the data can still be recovered with the use of a parity stripe. Briefly, this is stated on page 11, beginning on line 16 in the definition of striper where the parity stripe is referred to, as well as line 28 where the parity stripe is also referred to in regard to the unstriper.

As the specification states on page 10, beginning on line 25, in the switch architecture, all data is distributed evenly across all fabrics so the switch adds bandwidth by adding fabrics and the fabric need not increase its bandwidth capacity as a switch increases bandwidth capacity. What is key is the data is distributed evenly. That is, the data is not duplicated and 10 exact copies of the original received data is for instance sent to 10 fabrics, but the data or packet that is received is fragmented into 10 different parts, if there are 10

different fabrics, and the fragments are sent as stripes to the fabrics. The elements that accomplish this type of RAID architecture are described beginning on page 11, line 16 where there is referred a stripper, an unstriper, an aggregator and so on. Thus, to one skilled in the art, it is second nature that when RAID techniques are identified, stripping of fragments of packets will be known in the general sense. Where the novelty and uniqueness begins in regard to the claimed invention is its application to a switching environment regarding packets, where RAID techniques are commonly used in the prior art with respect to video servers. Accordingly, it is respectfully submitted that where the Examiner is looking for the exact combination of words to be found present in the specification, in fact the clear and implied intent and the teachings from the specification in regard to RAID techniques indicates to one skilled in the art that striping is occurring and is occurring of the fragments bad.

It is further clear from the description of the preferred embodiment beginning on page 8, line 7, that the purpose of the gigabit transceivers that make the connections from the port cards 12 to fabrics 20 across the back plane is to facilitate the transfer of the different stripes of fragments. In fact, substitute figure 6 shows the timing necessary to make sure that while the stripes of corresponding fragments are sent to different fabrics, a sync pulse is used to synchronize the various fabrics so that when the corresponding fragments are reviewed at any given time, it is known which fragments align with the other fragments at a corresponding time so that the data can be reformed.

The Examiner has rejected Claims 1-13 and 15-17 under 35 U.S.C. 112, second paragraph. In regard to Claim 1, the Examiner states it is not clear "stripes been of fragments" means. It is respectfully submitted by applicants that they have explained what stripes of fragments means above in regard to the rejection under 35 U.S.C. 112, first paragraph.

In regard to Claims 4 and 15 and a the terminology "240 G slow" and "240 G fast", the terminology "240 G slow" refers to a speed up of 1 and "240 G fast" refers to a speedup of 2. A speedup of 2 means that the interface or port card receives data at a rate two times as fast as it can send data out. A speedup of one simply means that it can receive the same amount of data as it can send out.

In regard to Claim 12, it has been amended so that the word "networks" refers to the "network" referred to previously. The network that is referred to has to do with the interconnections between the interface or port cards and the fabrics of the switch. It is respectfully submitted one skilled in the art from reading the specification of the above-identified patent application would understand the language of Claims 4, 12 and 15.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-13 and 15-17, now in this application be allowed.

CERTIFICATE OF MAILING

I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 6/11/99

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